



IEEE PROJECT CENTER 2016 TITLES

VLSI Projects

Sl.No	VLSI Titles
IEEEVLSI201601	A Fully Digital Front-End Architecture for ECG Acquisition System With 0.5 V Supply
IEEEVLSI201602	A High-Speed FPGA Implementation of an RSD-Based ECC Processor
IEEEVLSI201603	A Mixed-Decimation MDF Architecture for Radix-2K Parallel FFT
IEEEVLSI201604	Algorithm and Architecture of Configurable Joint Detection and Decoding for MIMO Wireless Communications With Convolution Codes
IEEEVLSI201605	One-Cycle Correction of Timing Errors in Pipelines With Standard Clocked Elements
IEEEVLSI201606	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels
IEEEVLSI201607	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication
IEEEVLSI201608	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding
IEEEVLSI201609	RF Power Gating A Low-Power Technique for Adaptive Radios
IEEEVLSI201610	Hardware and Energy-Efficient Stochastic LU Decomposition Scheme for MIMO Receivers
IEEEVLSI201611	A Configurable Parallel Hardware Architecture for Efficient Integral Histogram Image Computing
IEEEVLSI201612	Hybrid LUT/Multiplexer FPGA Logic Architectures
IEEEVLSI201613	A 520k (18 900, 17 010) Array Dispersion LDPC Decoder Architectures for NAND-Flash Memory
IEEEVLSI201614	Implementing Minimum-Energy-Point Systems With Adaptive Logic
IEEEVLSI201615	High-Performance Pipelined Architecture of Elliptic Curve Scalar Multiplication Over GF(2 ^m)
IEEEVLSI201616	A New Binary-Halved Clustering Method and ERT Processor for ASSR System
IEEEVLSI201617	High-Performance NB-LDPC Decoder With Reduction of Message Exchange
IEEEVLSI201618	Low-Power ECG-Based Processor for Predicting Ventricular Arrhythmia
IEEEVLSI201619	LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter
IEEEVLSI201620	Graph-Based Transistor Network Generation Method for Supergate Design
IEEEVLSI201621	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic
IEEEVLSI201622	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers
IEEEVLSI201623	A 0.52/1 V Fast Lock-in ADPLL for Supporting Dynamic Voltage and Frequency Scaling
IEEEVLSI201624	Source Code Error Detection in High-Level Synthesis Functional Verification



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IEEEVLSI201625	A Cellular Network Architecture With Polynomial Weight Functions
IEEEVLSI201626	Code Compression for Embedded Systems Using Separated Dictionaries
IEEEVLSI201627	A Dynamically Reconfigurable Multi-ASIP Architecture for Multi-standard and Multimode Turbo Decoding
IEEEVLSI201628	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications
IEEEVLSI201629	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks
IEEEVLSI201630	A New Parallel VLSI Architecture for Real-Time Electrical Capacitance Tomography
IEEEVLSI201631	The VLSI Architecture of a Highly Efficient De-blocking Filter for HEVC Systems
IEEEVLSI201632	Low-Power System for Detection of Symptomatic Patterns in Audio Biological Signals
IEEEVLSI201633	Low-Power FPGA Design Using Memorization-Based Approximate Computing
IEEEVLSI201634	Exploiting Intracell Bit-Error Characteristics to Improve Min-Sum LDPC Decoding for MLC NAND Flash-Based Storage in Mobile Device
IEEEVLSI201635	Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units
IEEEVLSI201636	Design and Implementation of High-Speed All-Pass Transformation-Based Variable Digital Filters by Breaking the Dependence of Operating Frequency on Filter Order
IEEEVLSI201637	Unequal-Error-Protection Error Correction Codes for the Embedded Memories in Digital Signal Processors
IEEEVLSI201638	A High Throughput List Decoder Architecture for Polar Codes
IEEEVLSI201639	A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO
IEEEVLSI201640	Design and FPGA Implementation of a Reconfigurable 1024-Channel Channelization Architecture for SDR Application
IEEEVLSI201641	A Single-Ended With Dynamic Feedback Control 8T Sub threshold SRAM Cell
IEEEVLSI201642	A Low-Power Robust Easily Cascaded Penta MTJ-Based Combinational and Sequential Circuits
IEEEVLSI201643	OTA-Based Logarithmic Circuit for Arbitrary Input Signal and Its Application
IEEEVLSI201644	A Robust Energy/Area-Efficient Forwarded-Clock Receiver With All-Digital Clock and Data Recovery in 28-nm CMOS for High-Density Interconnects
IEEEVLSI201645	Low-Power Variation-Tolerant Nonvolatile Lookup Table Design



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IEEEVLSI201646	Full-Swing Local Bitline SRAM Architecture Based on the 22-nm FinFET Technology for Low-Voltage Operation
IEEEVLSI201647	High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator
IEEEVLSI201648	A 0.1–3.5-GHz Duty-Cycle Measurement and Correction Technique in 130-nm CMOS
IEEEVLSI201649	Low-Energy Power-ON-Reset Circuit for Dual Supply SRAM
IEEEVLSI201650	Frequency-Boost Jitter Reduction for Voltage-Controlled Ring Oscillators